REMARKS

Claims 1-26 were originally pending in this application. On June 22, 2005, Applicant responded to a restriction requirement by electing to withdraw claims 11, 12, and 20-26. Claims 1-10 and 13-19 are currently pending. The Office has rejected claims 1-10 and 13-19 under 35 USC § 103(a) as being unpatentable over Asahi (U.S. Pat. No. 6,975,516) in view of Smith et al. (U.S. Pat. No. 6,340,796; hereinafter "Smith"). This is a non-final Office action and is responsive to Applicant's communication filed on or about April 10, 2006.

103(a) Rejection of Independent Claims 1 and 13

Asahi does not show or suggest "an embedded discrete surface mount first decoupling capacitor mounted to the outer surface of the first reference plane layer, the first decoupling capacitor comprising a first electrode connected to the first reference plane and a second electrode connected to the second reference plane," as required by Applicant. The Office asserts that figure 8 of Asahi discloses these elements. The Office copied figure 8 from Asahi into Appendix "A" of the Office action and added callouts not present in the figure, as disclosed by Asahi. The Office added four callouts (804-1a, 804-2a, 804-1b, and 804-2b), each pointing to a different object. Additionally, there are three other objects (804, 810, and 812) in figure 8 that are labeled by Asahi. Asahi describes these three objects (804, 810, and 812) as simply electronic components. (Col. 12, lines 8-33.) Nowhere in the description of any of the objects found in figure 8 is the term capacitor used. Furthermore, Asahi does not specifically describe the objects (804-1a, 804-2a, 804-1b, and 804-2b) labeled by the Office in Appendix "A". Absent a specific description of the objects by Asahi, it is improper for the Office to assign a description without at least providing an explanation for how it arrived at the assignment. Even if hypothetically, the objects (804-1a, 804-2a, 804-1b, and 804-2b) are the same as the labeled objects (804, 810, and 812), Asahi described them as simply electronic components. Applicant requires an embedded discrete surface mount decoupling capacitor. This element is missing from Asahi.

Applicant requires the electrodes, of each of the embedded discrete surface mount decoupling capacitors, to be attached to reference planes. A person of ordinary skill in the art would understand that the term "reference plane" refers to a power or ground plane. The Office asserts that an object 808 shown in figure 8 embodies this requirement. Applicant disagrees. Asahi describes object 808 as a "three-layered wiring board" and depicts two instances of the three-layered wiring boards 808 in figure 8. (Col. 12, line 26.) In one of the depictions, Asahi describes the lower of the three layers 802 as a "wiring pattern." (Col. 12, lines 26-27.) Asahi is silent on the function of the other two layers that make up the three-layered wiring boards 808. In Appendix "A", the Office has labeled the top layer of one the boards 808 as a "First Reference Plane Layer" and the lower layer as a "Second Reference Plane Layer." There is no support in Asahi for this assertion by the Office. The layers, in the instance of three-layered wiring board 808 that the Office has labeled, are not described or labeled by Asahi. In the other instance of the three-layered wiring board 808, the lower layer is described as a wiring pattern 802, which is not the same as a reference layer. The other layers of this instance are not labeled and there is no teaching that any of the layers are indeed reference layers. The assertion by the Office that the top and lower layers are "reference layers" is unsupported by teachings of Asahi and therefore improper. Even if hypothetically they were reference layers, Asahi clearly shows the electrodes of the objects attached to the boards 808 are connected to each of the outer layers and the middle layer. To meet Applicants requirement that the electrodes are attached to reference planes, all three of Asahi's layers would have to be reference planes because Asahi's electrodes are connected to all three layers. This is not possible since Asahi clearly teaches that at least one of the three layers is a wiring pattern layer 802. Therefore, the Asahi fails to show or suggest at least these elements required by Applicant.

Smith teaches, "a printed wiring board structure interfaced with an integral core fabricated of a metal matrix with pitch based graphite fibers." (Col. 1, lines 8-10.) Smith fails to show or suggest the above elements missing from Asahi.

At least these elements, required by Applicant, are missing from the prior art references. Thus, the Office has failed to establish a *prima facie* case of obviousness. The rejection is improper and the claims are allowable over the prior art made of record.

103(a) Rejection of the Dependent Claims

Claims depending from claims 1 and 13 are allowable for at least the same reasons presented above.

CONCLUSION

Applicant asks that the Office reconsider this application and allow all pending claims. Please charge any fees that might be due, excluding the issue fee, to deposit account 14-0225.

Respectfully submitted,

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(Electronically Filed)

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